Method and arrangement for concealing errors

This invention relates to a method for concealing errors in a digital information signal. Such method is e.g. known from US-patent 5.715.312.

Usually, when a digital information signal is stored on a storage medium, the storage medium also comprises an error correction code, which makes the retrieval from the medium more robust against possible errors in the information signal. However, sometimes the error correction fails and then the remaining failures may extend for at least one frame or a number of frames. Such failure will, because of its duration of e.g. 1/75 sec. or more, be very troublesome. The technique of error concealment seeks to replace the damaged area of the signal by a signal from a neighbouring undamaged frame.

The present invention has for its object to provide a method for concealing errors in a single bit bitstream signal. Such signal format is e.g. adopted for the Super Audio Compact Disc (SA-CD) and the method according to the invention is therefore characterized in that the digital information signal is a single bit bitstream and that the method comprises low pass filtering the single bit bitstream for constructing the low frequency contents of the single bit bitstream, interpolating the low frequency contents during an error using low frequency contents before and/or after the error and converting the low frequency signal obtained after the interpolating into a regenerated single bit bitstream with concealed errors by means of a $\Sigma\Delta$-modulator.

This method results in a cheap and easy to implement error concealment of single bit digital signals. However, the quality standard is not very high. The method implies that a signal, which is once quantized in a $\Sigma\Delta$-modulator, is requantized in a second $\Sigma\Delta$-modulator. Especially at the higher signal frequencies, which are still of importance for the faithful reproduction of the signal (e.g. about 100 kHz in case of audio-signals), multiple quantization causes such deterioration of the signal quality that highest quality standards are not anymore fulfilled. In order to avoid such deterioration of the signal quality, the method according to the invention may further be characterized by outputting the received single bit bitstream during the absence of an error and outputting the regenerated single bit bitstream

during the occurrence of an error and by bit-synchronizing the ΣΔ-modulator to the received single bit bitstream. When a single bit bitstream is low pass filtered and then remodulated into a second single bit bitstream, the two bitstreams are not any more identical so that switching between the two bitstreams causes audible clicks. To avoid these clicks the two bitstreams have to be bit-synchronized in order to ensure that the two bitstreams are, substantially, equal around the moments of switching. Suitable methods of bit-synchronizing two bitstreams are disclosed in applicants copending European patent application...(ID 602604).

The invention also relates to an arrangement for carrying out the above described methods. Such arrangement may be characterized in that it comprises in cascade a low pass filter for constructing the low frequency contents of the single bit bitstream, means for replacing the low frequency contents during an error by a low frequency approximation of the signal and a ΣΔ-modulator for converting the low frequency signal obtained after the replacement into a regenerated single bit bitstream with concealed errors. The arrangement may preferably be further characterized by switching means applying the received single bit bitstream to an output terminal during the absence of an error and applying the regenerated single bit bitstream to the output terminal during the occurrence of an error and means for synchronizing the ΣΔ-modulator to the received single bit bitstream.

The invention will be further explained with reference to the attached figures. Herein shows:

Figure 1 a schematic diagram of a first arrangement according to the invention and

Figure 2 a schematic diagram of a second arrangement according to the invention.

The arrangement of figure 1 comprises a compact disc storage unit S from which the stored information signal is obtained. This signal, which is a single bit digital signal in compressed format, is decompressed in decompressor unit D. This unit also performs error correction on the received signal, so that at its output a corrected and uncompressed single bit bitstream is obtained. The unit D also provides an error flag EF to identify those portions of the signal where the error correction failed and which portions have to be concealed in order to avoid or minimize audible distortions.

The single bit bitstream x(n) obtained from the decompressor unit D is e.g. a stream of +1 and -1 bits at a rate of 64 x 44,1 kHz and the mean value of which represents the useful low frequency (audio) information. This information is extracted from the bitstream by a digital low pass filter F, which is preferably of fifth order and which has a cut off frequency of about 100 kHz. This low frequency signal is fed to a unit I which is controlled by the error flag EF and which replaces, during an error, the damaged part of the signal by a reconstruction of the original signal which may be obtained by interpolation. The interpolation is preferably done so, that with the undamaged parts of the signal discontinuities in the signal level are avoided. A useful method of interpolation is e.g. the harmonic retrieval method which is described in the article: "Model Based Processing of Signals: A State Space Approach" of B.D. Rao and K.S. Arun in Proceedings of the IEEE Vol 80 , No 2 p.p. 283-309, 1992. Subsequently the repaired LF-signal u(n) is converted to a new single bit bitstream y(n) by means of a ΣΔ-modulator SD.

The low pass filter F has the object to free the input of the ΣΔ-modulator from too large high frequency signal components. The large HF signal components of the single bit bitstream would otherwise cause the ΣΔ-modulator to malfunction and become unstable. For this reason it would be wise to choose the cutoff frequency of the low pass filter as low as possible e.g. at about the highest audible frequency of 20 kHz. However, it has been found that the frequencies between 20 kHz and 100 kHz, although not audible per se, still contribute to the fidelity of the sound perception. For this reason the cutoff frequency of the low pass filter F is preferably chosen at about 100 kHz. On the other hand, these higher LF frequencies have the disadvantage that they cause some distortion (noise) in the ΣΔ-modulator SD. Therefore it is advisable to avoid that the signal, which has already been converted to a single bit bitstream prior to its storage on the storage medium S, is converted a second time into a single bit bitstream. This is the object of the arrangement of figure 2.

In this arrangement elements, which correspond with those of figure 1, have been given corresponding references and need no further explanation. Additionally, this arrangement comprises a switch SW which is controlled by the error flag EF and which connects the original bitstream x(n) from the unit D directly to the output O when there is no error. On the other hand, when the error flag is set, the switch SW connects the output of the ΣΔ-modulator SD to the output O. Therefore, reconversion of the original bitstream into a second bitstream is avoided.

In the arrangement of figure 2 measures have to be taken to ensure that the switching over from the original bitstream x(n) to the bitstream y(n) of the ΣΔ-modulator SD and vice versa does not cause audible clicks. These clicks would normally occur because the bits of the two bitstreams will usually not be equal, even when they carry exactly the same LF information. Therefore it is necessary to synchronise the bitstream y(n) of the ΣΔ-modulator to the received bitstream x(n) from the unit D. To this end, the arrangement of figure 2 comprises a synchronizing unit SU which receives the information of the original bitstream x(n) from unit D and the digital LF input signal u(n) of the ΣΔ-modulator and which generates a correction signal ε for application to one or more of the integrator states inside the ΣΔ-modulator. As already described in applicants copending European patent application (ID 602604) it is achieved by this measure that, after a certain number of bits, the bitstream of the ΣΔ-modulator runs substantially synchronously with the original bitstream. As an example: prior to the switching over from the original bitstream to the bitstream of the ΣΔ-modulator, the ΣΔ-modulator is synchronised to the original bitstream during about 5000 bits, then the switch SW supplies about 40000 bits of the ΣΔ-modulator to the output O, then, when the error flag is reset, the switch SW remains during 5000 bits connected to the ΣΔ-modulator until the ΣΔ-modulator is again synchronised to the original bitstream and then the switch reconnects the output O to this original bitstream.

It is noted that the computational effort of the interpolator I is intensive because it has to be done at run time. To simplify or avoid the interpolation, the storage medium S may comprise, in a special area somewhere on the storage medium, a highly compressed image of the data stored normally on the medium. This highly compressed image is applied to the unit I through a dotted line HC and can be used to assist or replace the normal interpolation calculations. The same measure may be taken in the arrangement of figure 1.